REMARKS

Claims 1–20 are pending in the present application.

The specification has been amended to delete Figures 4A and 4B and remove all references thereto, and to revise the description for consistency following such deletion.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Enablement)

Claims 7, 8 and 15-20 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. This rejection is respectfully traversed.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-195 (8th ed., rev. 3, August 2005). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *Id.* A patent need not teach, and preferably omits, what is well known in the art. *Id.* The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04 at 2100-197. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

The Office Action objects to the limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" in claims 7 and 15. As previously noted, it was well-known in the art at the time the instant application was filed that a global or "system" clock may be used to coordinately control various components or logical units within an integrated circuit. Such signals are understood to exists and generally are NOT depicted in high level drawings (e.g., functional unit drawings, as opposed to circuit diagrams). Thus, those skilled in the art would not be confused by the absence of a expressly depicted system clock signal within a functional drawing of an integrated circuit.

The Office Action concedes that the absence of an expressly depicted system clock signal within a functional drawing of an integrated circuit would not confuse those skilled in the art. Paper No. 09102005, pages 6–7. However, the Office Action asserts that it is unclear as to how the pulsed biased current is generated from the system clock, and suggests that it would require undue experimentation for those skilled in the art to produce a pulse generator capable of generating a pulsed current bias. Applicant respectfully notes that such an assertion is wholly contradictory with the assertion in the Office Action that current Ib in U.S. Patent No. 5,841,306 to *Lin et al* comprises a pulsed bias current.

The Office Action objects in particular to the limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock." At the time the application was filed, clock signals were well

known to have rising and falling edges, and use of a clock edge to trigger an event or action ("edge-triggered") was also well-known. As previously noted by the Applicant, paragraph [0029] of the application (copied below with emphasis added) clearly demonstrates support for generating a pulsed biased current from the system clock:

> [0029] A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 μs bias current pulse. Transistors within comparator 100 are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before the falling edge of the system clock (clk) signal, where the system clock period is 20 μs and the clock duty cycle is 50%. *The pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge.*

The above-reference paragraph describes how the pulsed bias current (in the exemplary embodiment) includes a pulse on the falling edge of the system clock and sampling a comparator output on the rising edge of the system clock. Moreover, the above-referenced paragraph not only describes how the pulse bias current is produced (in an exemplary embodiment), but also provides specific requirements for the comparator (which influences the output of the comparator). For example, paragraph [0029] specifies for this exemplary embodiment that a pulsed generator be coupled to the comparator and produces a 390 μs bias current pulse. Transistors within the comparator are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs.

In addition, Applicant respectfully notes that the assertion within the Office Action that those skilled in the art would be required unduly experiment in order to generate edge-triggered signals

is wholly contradictory with the assertion in the Office Action that current Ic3 in U.S. Patent No. 6,323,695 to *Heinrich* has the pulse shaped current.

The application as filed adequately enables generating a pulsed biased current, and triggering the pulse bias current on one edge of the system clock while sampling an output of the comparator on the other edge. Accordingly, no undue experimentation would be required for those skilled in the art to implement such features as required by the claims.

The Office also objects to the limitations "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value" in claim 8, "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current" in claim 16, and "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current" in claim 17. Specifically, the Examiner contends that it is unclear as to how the circuit shown in Figures 4A and 4B enable operation in a first and second mode:

> Page 11, lines 6–25; page 12, lines 1–25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the circuit shown in figures 4A and 4B enable operatively in first and second modes** as called for in claim 8. That is, it is unclear as to how the comparator is selected to operate in a first mode in which the input gain

> stage is biased by a bias current with a defined first level value or when the comparator is selected to operate in a second mode the input gain stage is biased a bias current with a different second level value without undue experimentation.

Paper No. 09102005, page 3 (emphasis in original). As previously noted, paragraph [0023] of the application as filed states:

> [0023] In an i_power_low_speed mode (or "low power comparator" configuration), the quiescent current of the amplifier (first gain stage 101) is driven with a constant bias current of ibias/6, so that comparator 100 has low power consumption but a long propagation delay slow_prop. In an i_power_high_speed mode (or "fast comparator" configuration), the quiescent current of the amplifier is driven with a constant bias current of 5*ibias, such that comparator 100 has higher power consumption but a faster propagation delay fast_prop.

The application clearly describes the implementation of different modes and different current levels for a functional unit. The exemplary embodiment in Figure 2A depicts the timing diagram of operation in a low speed mode, while Figures 2B and 2C depict the timing diagrams of operation in a high speed mode. Each mode is driven by different bias current values. For example, when the current in the first gain stage 101 is driven with a constant bias current of ibias/6, the comparator will generally operate in a low speed mode. On the other hand, when the current in the first gain stage 101 is driven with a constant bias current of 5* ibias, then the comparator will generally operate in a high speed mode. Applicant's Specification, ¶ [0023], pp. 10-11. The application thus adequately enables selective operation of a comparator in a first mode and in a second mode. The fact that the feature is not ALSO enabled by the partial circuit diagrams of Figures 4A and 4B is irrelevant.

The Office Action further objects to the limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal" in claim 19. The Office Action states:

> Figure 1 shows "**an equivalent circuit**" of the actual present invention. The equivalent circuit shows a symbol of a variable current (ibias) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification use waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the current source being biased by the pulse of continuous bias current and controlled by the input current would correspond to the actual components of the actual comparator shown in figures 4A and 4B.**

Paper No. 09102005, pages 3–4 (emphasis in original). Figure 1 depicts, within the first (input) gain stage 101, a current source I1 producing bias current ibias and controlled by pulsed transconductance signal gm. These features are similar to the corresponding features of Figure 5 as filed (now Figure 4), illustrating known integrated circuit comparators. Moreover, the application as filed states:

> [0016] FIGURE 1 depicts an equivalent circuit diagram for a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. Comparator circuit 100 is formed within an integrated circuit device and includes a differential input pair V(inp) and V(inn) producing a pulsed transconductance gm received as an input by a first gain stage 101. The pulse input changes the bias current Ibias from the current source I1, changing the bias current of the whole comparator 100.
> [0017] The first gain stage 101 includes an output resistance go and output capacitance (including Miller capacitance) Cp in parallel with the current source I1. Connected to the output of the first gain stage 101 is a voltage limiter 102 and a built-in hysteresis circuit 103 including a current source I2 driven by a hysteresis current signal Ihys that is switched into and out of parallel connection with the first gain stage 101 at the output of the first gain stage 101 based on the comparator's output voltage out. Connected between the output of the first gain stage 101 (and to hysteresis circuit 103) is a second gain stage 104 including a current source I3 driven by a gain signal A2*ngain.

The structures depicted in the equivalent circuit diagram of Figure 1 may be readily implemented by those skilled in the art, such that no undue experimentation would be required for those skilled in the art to implement the features recited in claim 19.

Therefore, the rejection of claim 7, 8 and 15–20 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1–3, 10 and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,841,306 to *Lim*. Claims 1–3, 8–11, 16 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,323,695 to *Heinrich*. These rejections are respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 3, August 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

As previously noted, independent claims 1 and 9 each recite an input gain stage biased with a pulsed bias current. Such a feature is not found in the cited references. *Lim* teaches a bias control unit 10 controlling whether or not bias current is provided to comparator 20, providing bias current

in an operating mode and not providing bias current during a power-saving mode as determined by the state of a mode control "trigger" input signal Vtri. However, *Lim* does not teach providing a pulsed bias current – that is, a current that is pulsed in accordance with a system clock – rather than a continuous bias current. Merely preventing the bias current from being supplied during periods when the comparator is not needed in order to reduce power consumption (as in the low power mode disclosed in the instant application) does not constitute provision of a "pulsed" bias current (one that is alternately on and then off during each clock cycle) rather than a continuous bias current.

The Office Action states:

> Regarding claims 1-3 and 10-11 as being anticipated by Lim (USP 5,841,306), applicant argues that Lim does not show input gain stage biased with a pulsed bias current as called for in claims 1-3 and 10-11 is no persuasive. Figure 5C of Lim clearly shows the bias current Ib as a pulse current biasing the input gain stage in figure 4. Therefore, the rejection is deemed proper.

Paper No. 09102005, page 8. However, as previously noted, a "pulsed" bias current as used in the specification is one that is pulsed (turn on and then turned off) during each cycle of the system clock:

> [0006] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide, for use in an integrated circuit comparator, ***a pulsed rather than continuous bias current applied, in at least a fast comparator configuration, to a current source within a comparator's input gain stage***. The transconductance current will then be pulsed rather than continuous. ***The pulse width of the bias current is small relative to the system clock***, but has a large current magnitude allowing the comparator to quickly respond to applied voltages. The end result is a fast comparator but without the large quiescent current associated with conventional fast comparators. A voltage limiter optimizes the ngain node voltage excursion. A built-in hysteresis circuit suppresses any spurious voltage spikes at the output node at every comparator's bias pulse. ***The bias current pulse and sampling of the comparator occur in predefined relation to the system clock***.

Specification, ¶ [0006] (emphasis added). In the exemplary embodiment, the specification teaches that the bias pulses have a duration of 390 nanoseconds (0.39 microseconds) while the system clock period is 10 microseconds, for a bias current duty cycle of 3.9%. Specification, ¶¶ [0026]-[0027]. The specification thus makes clear that "pulsed" is used to indicate that the bias current is "on" during only a portion of each clock cycle, as opposed to "continuous" bias current in which the bias current is on during the entire clock cycle, as depicted by the transconductance signal gm in Figure 1:

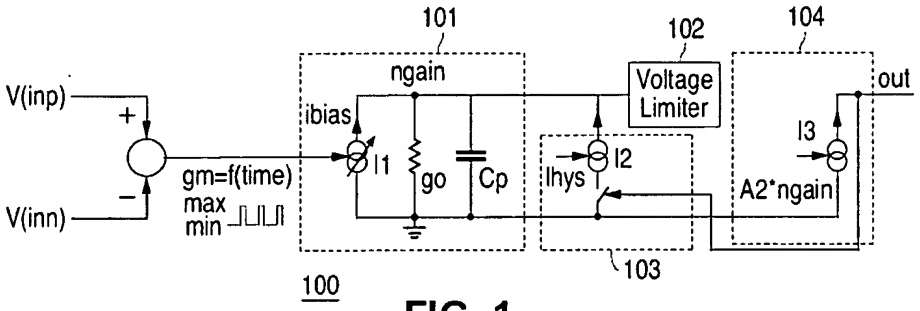
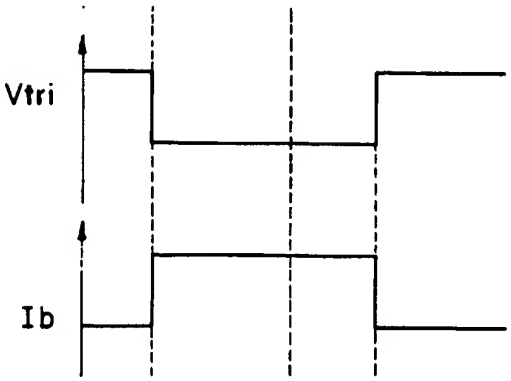


FIG. 1

By contrast, *Lim* depicts a current Ib that is turned on (by trigger signal Vtri depicted in Figure 5B) when the comparator is needed and turned off when the comparator is no longer needed (also by trigger signal Vtri depicted in Figure 5B):

FIG. 5B

FIG. 5C



While the system clock is not depicted in *Lim* (as conventional), it is understood that the period during which current Ib is "on" encompasses multiple clock cycles. As previously noted, this is analogous to the low power mode operation of the present invention, in which a continuous bias current is provided, but only when the comparator is "enabled":

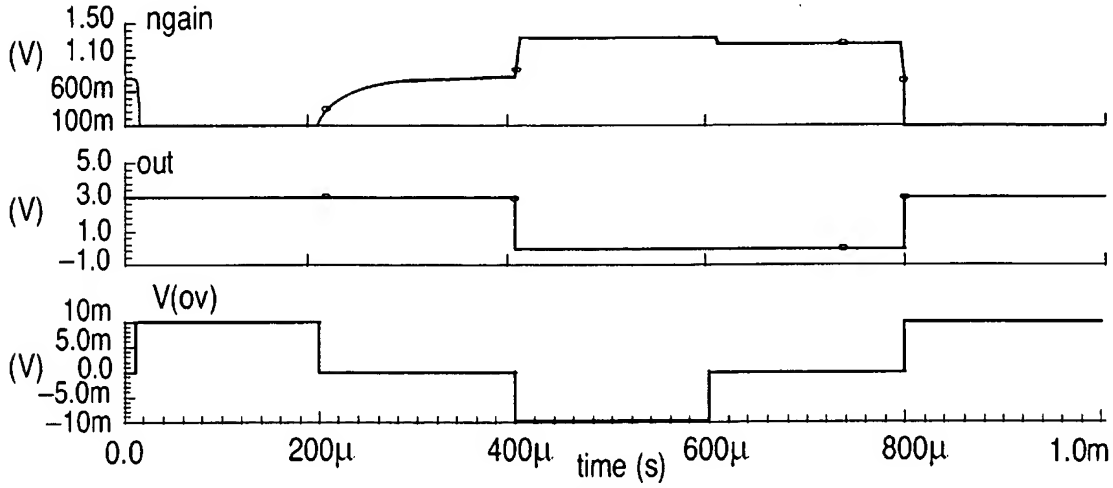


FIG. 2A

In the low power embodiment of the present invention, the comparator is effectively disabled (output voltage goes to zero) when the overdrive voltage V(ov) – the counterpart in the present invention to the trigger voltage Vtri in *Lim* – reaches a predetermined level. The comparator is similarly disabled during operation with a pulsed bias current:

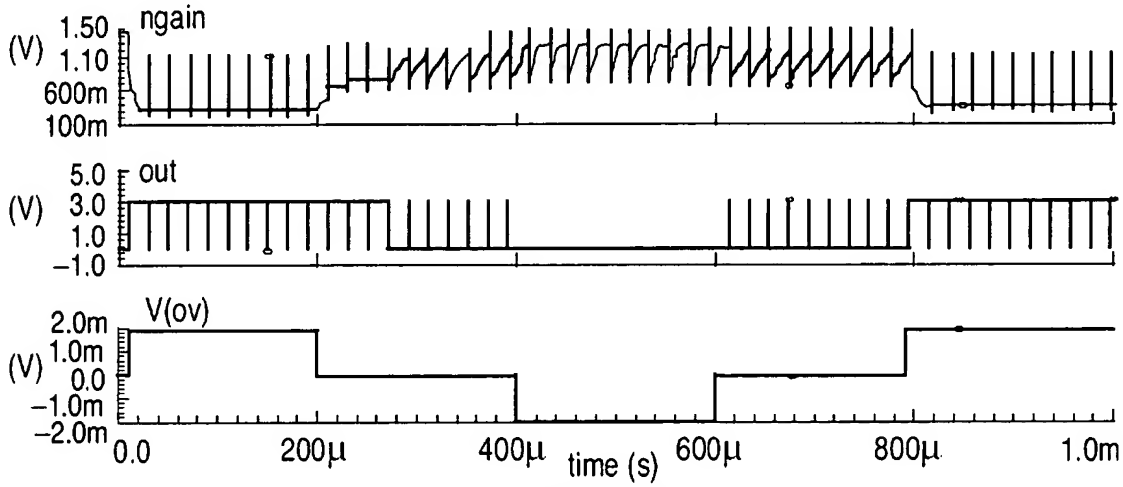


FIG. 2C

The use of a pulsed bias current while a comparator is operational is thus distinct from disabling the comparator when not needed, as disclosed in both *Lim* and the specification. The current Ib "pulse" in *Lim* is thus NOT a "pulsed" bias current as that term is employed in the specification and claims of the present application, and *Lim* does not anticipate the pending claims.

As previously noted, *Heinrich* similarly teaches providing a continuous bias current Ic at varying levels depending on an operating mode (i.e., whether the input signal is constant or varying):

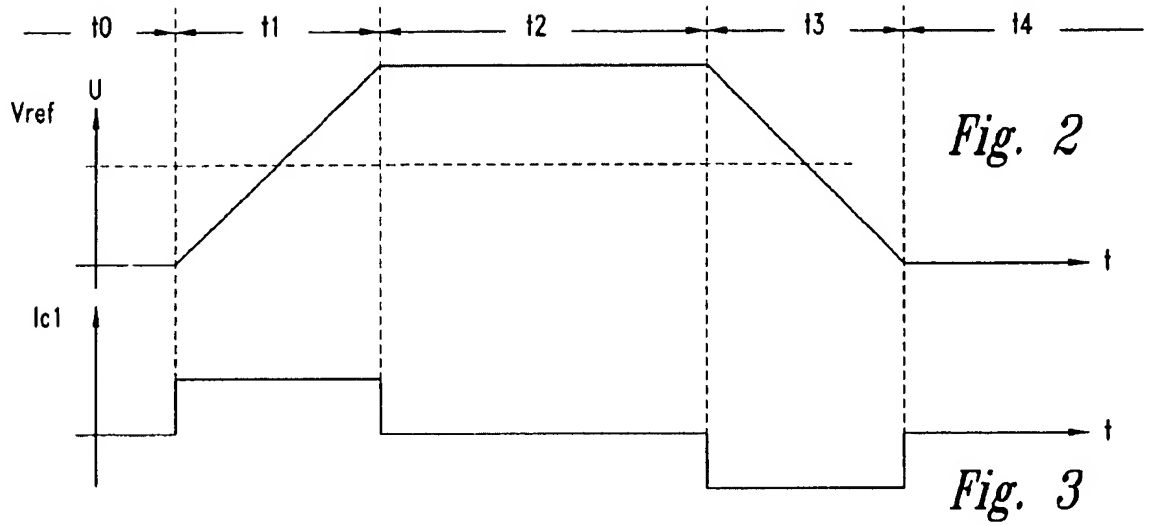


Fig. 2

Fig. 3

In particular, *Heinrich* does not even state that the current Ic1 is ever turned off, but instead merely teaches that the magnitude of current Ic1 varies between different levels. Again, this is analogous to the provision of different magnitude (ibias/6 or 5*ibias) continuous bias currents as disclosed in the present invention, which also distinct from providing a pulsed bias current. Merely altering levels for the bias current does not comprise pulsing the bias current. In that regard, the Office Action states:

> Regarding the rejection claims 1-3, 8-11 and 16-17 as being anticipated by Heinrich (USP 6,323,695), applicant argues that Heinrich does not show pulsed bias current as called for in claims 1-3, 8-11 and 16-17 is not persuasive. The current Ic1 in figure 3 having a pulse shape waveform anticipating the limitations called for in claims 1-3, 8-11 and 16-17. Therefore, the rejection is deemed proper.

Paper No. 0910-2005, page 9. The Examiner's insistence on adopting an interpretation of the claim term "pulsed bias current" any bias current that can be characterized as having the shape of a pulse

is inconsistent with the specification, drawings and claims as filed, and is therefore arbitrary and capricious. Moreover the interpretation adopted by the Examiner has effectively been disclaimed by the Applicant during prosecution. Nonetheless, Applicant affirmatively asserts for the record that the term "pulsed bias current" as used in the specification and claims refers to a bias current that is only active for a portion of each clock period for the system clock of the integrated circuit within which the claimed comparator is implemented.

As previously noted, independent claim 17 recites that the input gain stage bias current is selectively either pulsed or continuous (constant). Such a feature is not shown in the cited references.

Therefore, the rejection of claim 1–3, 8–11 and 16–17 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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